WHAT IS CLAIMED IS:

1. A common voltage regulating circuit of a liquid crystal display device, comprising:

a pulse signal generating means for outputting a pulse width modulation signal in response to up/down signal for adjusting a common voltage;

a smoothing means for smoothing the pulse width modulation signal from the pulse signal generating means to a direct current level; and

an amplifying means for amplifying the signal smoothed by the smoothing means to a predetermined level and outputting a common voltage signal.

2. The common voltage regulating circuit of a liquid crystal display device according to claim 1, wherein the smoothing means includes a third resistor for receiving the pulse width modulation signal through one end and a first capacitor coupled between the other end of the third resistor and a ground.

3. The common voltage regulating circuit of a liquid crystal display device according to claim 1, wherein the amplifying means includes a fourth resistor coupled between

an inverting terminal and an output terminal, a fifth resistor coupled between the inverting terminal and a ground, and a non-inverting amplifier for receiving the signal smoothed by the smoothing means through a non-inverting terminal and amplifying the receive signal to a predetermined level in order to output the common voltage signal.

4. A common voltage regulating circuit of a liquid crystal display device, comprising:

a data generating means for outputting a synchronizing signal and a serial digital data signal in response to an up/down signal for adjusting a common voltage;

a digital/analog converting means for converting the serial digital data signal into an analog signal in response to the synchronizing signal of the data generating means; and

a buffer amplifying means for buffering the analog signal converted by the digital/analog converting means and then outputting a common voltage signal.

5. The common voltage regulating circuit of a liquid crystal display device according to claim 4, wherein the buffer amplifying means includes a buffer amplifier and a second capacitor, wherein the buffer amplifier feedbacks the common voltage signal to an inverting terminal, receives the

analog signal converted by the digital/analog converting means through a non-inverting terminal, buffers the analog signal and then outputs the common voltage signal, and wherein the second capacitor is coupled between an output terminal and a ground in order to remove an alternating current component.

6. A common voltage regulating circuit of a liquid crystal display device, comprising:

a data generating means for outputting a synchronizing signal and a parallel digital data signal in response to an up/down signal for adjusting a common voltage;

a digital/analog converting means for converting the parallel digital data signal into an analog signal in response to the synchronizing signal of the data generating means; and

a buffer amplifying means for buffering the analog signal converted by the digital/analog converting means and then outputting a common voltage signal.

7. The common voltage regulating circuit of a liquid crystal display device according to claim 6, wherein the buffer amplifying means includes a buffer amplifier and a third capacitor, wherein the buffer amplifier feedbacks the

common voltage signal to an inverting terminal, receives the analog signal converted by the digital/analog converting means through a non-inverting terminal, buffers the analog signal and then outputs the common voltage signal, and wherein the third capacitor is coupled between an output terminal and a ground in order to remove an alternating current component.

8. A common voltage regulating circuit of a liquid crystal display device, comprising:

a data storage means for receiving a first selection signal, a second selection signal, a synchronizing signal and a serial digital data signal in order to adjust a common voltage, and storing and outputting the synchronizing signal and the serial digital data signal according to a combination of the first selection signal and the second selection signal;

a digital/analog converting means for converting the serial digital data signal outputted from the data storage means into an analog signal in response to the synchronizing signal provided from the data storage means in an output mode of the data storage means, and converting a serial digital data signal inputted from an outside into an analog signal in response to a synchronizing signal inputted from an outside

in inhibition of write and output mode of the data storage means; and

a buffer amplifying means for buffering the analog signal converted by the digital/analog converting means and then outputting a common voltage signal.

9. The common voltage regulating circuit of a liquid crystal display device according to claim 8, wherein, when the first selection signal and the second selection signal are disabled, the data storage means is in a state in which both writing and reading are inhibited.

10. The common voltage regulating circuit of a liquid crystal display device according to claim 8, wherein, when the first selection signal is disabled and the second selection signal is enabled, the data storage means is in a state in which only writing can be performed.

11. The common voltage regulating circuit of a liquid crystal display device according to claim 8, wherein, when inputs of the first selection signal, the second selection signal, the synchronizing signal and the serial digital data signal are opened, the data storage means is in a state in which only outputting can be performed.

12. The common voltage regulating circuit of a liquid crystal display device according to claim 8, wherein the buffer amplifying means includes a buffer amplifier and a fourth capacitor, wherein the buffer amplifier feedbacks the common voltage signal to an inverting terminal, receives the analog signal converted by the digital/analog converting means through a non-inverting terminal, buffers the analog signal and then outputs the common voltage signal, and wherein the fourth capacitor is coupled between an output terminal and a ground in order to remove an alternating current component.

13. The common voltage regulating circuit of a liquid crystal display device according to claim 4 or 8, wherein the number of the bit of the serial digital data signal can be adjusted to be a value higher than deviation range of the common voltage signal.

14. A common voltage regulating circuit of a liquid crystal display device, comprising:

a data storage means for receiving a first selection signal, a second selection signal, a synchronizing signal and a parallel digital data signal in order to adjust a common

voltage, and storing and outputting the synchronizing signal and the parallel digital data signal according to a combination of the first selection signal and the second selection signal;

a digital/analog converting means for converting a parallel digital data signal inputted from an outside into an analog signal in response to a synchronizing signal inputted from an outside in inhibition of write and outpute mode of the data storage means, and converting the parallel digital data signal outputted from the data storage means into an analog signal in response to the synchronizing signal provided from the data storage means in outputting mode of the data storage means; a buffer amplifying means for buffering the analog signal converted by the digital/analog converting means and then outputting a common voltage signal.

15. The common voltage regulating circuit of a liquid crystal display device according to claim 14, wherein, when both the first selection signal and the second selection signal are "L" state in a logic level, the data storage means is in a state in which both writing and reading are inhibited.

16. The common voltage regulating circuit of a liquid crystal display device according to claim 14, wherein, when the first selection signal is "L" state in a logic level and the second selection signal is "H" state in a logic level, the data storage means is in a state in which only writing can be performed.

17. The common voltage regulating circuit of a liquid crystal display device according to claim 14, wherein, when inputs of the first selection signal, the second selection signal, the synchronizing signal and the serial digital data signal are opened, the data storage means is in a state in which only outputting can be performed.

18. The common voltage regulating circuit of a liquid crystal display device according to claim 14, wherein, when both the first selection signal and the second selection signal are "low" state in a logic level, the digital/analog converting means receives a synchronizing signal and a parallel data signal inputted from an outside, and then generates an analog signal.

19. The common voltage regulating circuit of a liquid crystal display device according to claim 14, wherein the

buffer amplifying means includes a buffer amplifier and a fifth capacitor, wherein the buffer amplifier feedbacks the common voltage signal to an inverting terminal, receives the analog signal converted by the digital/analog converting means through a non-inverting terminal, buffers the analog signal and then outputs the common voltage signal, and wherein the fifth capacitor is coupled between an output terminal and a ground in order to remove an alternating current component.

20. The common voltage regulating circuit of a liquid crystal display device according to claim 6 or 14, wherein the bit number of the parallel digital data signal can be adjusted to be a value higher than deviation range of the common voltage signal.

21. A common voltage regulating circuit of a liquid crystal display device, comprising:

a data storage means for receiving a first selection signal, a second selection signal and a pulse width modulation signal, and storing and outputting the pulse width modulation signal according to a combination of the first selection signal and the second selection signal;

a smoothing means for smoothing a pulse width modulation

signal to a direct current level provided from an outside in test mode, and smoothing the pulse width modulation signal to a direct current level provided from the data storage means in write mode; and

an amplifying means for amplifying the signal smoothed by the smoothing means to a predetermined level and then outputting a common voltage signal.

22. The common voltage regulating circuit of a liquid crystal display device according to claim 21, wherein the smoothing means includes an eighteenth resistor which receives pulse width modulation signal from the storage means and an outside through one end, and a sixth capacitor which is coupled between the other end of the eighteenth resistor and a ground.

23. The common voltage regulating circuit of a liquid crystal display device according to claim 21, wherein amplifying means includes a nineteenth resistor which is coupled between an inverting terminal and an output terminal, a twentieth resistor which is coupled between the inverting terminal and a ground, and a non-inverting amplifier which receives the smoothed signal by the smoothing means through a non-inverting terminal, amplifies the smoothed signal to

predetermined level and outputs the common voltage signal.

24. The common voltage regulating circuit of a liquid crystal display device according to claim 1 or claim 21, wherein a duty ratio of the pulse width modulation signal is set as 50% so that an output of the common voltage signal can be an optimum value.

25. The common voltage regulating circuit of a liquid crystal display device according to claim 1 or claim 21, wherein a duty ratio of the pulse width modulation signal can be adjusted to be a value higher than the deviation range of the common voltage signal.